Joseph L Larabell

Computer Software Engineer

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ABOUT ME

Computer software engineer with background in hardware design (discrete level, not ASIC) specializing in Electronic Design Automation (EDA) applications.

US citizen currently residing in Tokyo, Japan. Willing to travel but not to relocate.

Native English fluency and reasonably OK in conversational-level Japanese (JLPT2).

EXPERIENCE

Siemens / Mentor Graphics (Principal Engineer)
2006 - present
Worked on coverage reporting and testplan tracking tools. Designed and implemented regression management and failure analysis products. Served as principal architect for client-server metrics-based verification tracking product.

Synopsys (Senior Applications Engineer)
1998 - 2006
Application support and home-office liason for VCS simulation products. Designed initial testbench architecture for key Vera customers. Designed and implemented a graphical stimulus editor as a one-off for a specific Vera customer.

Ikos Systems (Senior Software Engineer)
1996 - 1998
Designed and implementated Verilog-to-Ikos model translation product. Managed work on existing memory model generation product. Worked with CTO to create accelerator-based solutions for several corner-case simulation model scenarios.

Itochu Technoscience (Applications Engineer / Contractor)
1995 - 1996
Pre-sales and customer support for Ikos digital accelerator and Verilog/VHDL simulators. Implemented ASIC simulation cell and memory libraries for key customers.

Racal-Redac Japan (Manager, CAE Support)
1993 - 1995
Responsible for support and user migration for CADAT simulation product for Japanese customers after product end-of-life announcement. Provided liason between support staff in Japan and development staff in US/UK.

Racal-Redac / HHB Systems (Senior Systems Analyst)
1988 - 1993
Continued to support ASIC library generation tools (originally produced at FutureNet). Worked on major enhancements to CADAT digital simulatior including design of second-generation ASIC timing database schema.

Data I/O, FutureNet (Software Engineer)
1986 - 1988
Designed and implemented “Acculib” database-driven ASIC library generation tools. Supported CADAT simulator running on co-processor card for Windows platform.

United Technologies Lexar (Principal Member of the Programming Staff)
1985 - 1986
Bug fixes and enhancements to O/S for PBX system, including support for new disk-based file system.

United Technologies Lexar (Senior Design Engineer)
1982 - 1985
Designed and implemented cross-switch fiber-optic interface for PBX switch. Managed construction of the largest PBX switch the company ever sold as a one-off for a specific customer.

Transaction Technology, Inc (Design Engineer)
1981 - 1982
Designed and implemented memory controller for a 14-port memory subsystem to be used as part of a new banking back-office minicomputer system.

Magnavox, Inc, GPS Division (Design Engineer)
1980 - 1981
Designed memory / external interface card for a series of miltary GPS receivers.

Hughes Aircraft, Radar Systems (Member of the Technical Staff)
1978 - 1980
Designed microprocessor-controlled self-test board for radar signal processing system. Wrote regression tests for and debugged hardware issues in F15/F18 radar signal processor.

EDUCATION

Bachelor of Science, Electrical and Computer Engineering
1974 - 1978
Wayne State University, Detroit, Michigan USA
(Graduated Cum Laude, Member Tau Beta Pi)

SKILLS

Programming language Fluency: C, C++, Perl, Python, Java, JavaScript, Tcl/Tk, PL/M, Verilog, VHDL, Various assembly languages

CAD/CAE Tools: CADAT, Verilog-XL, Ikos, VCS, QuestaSim

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